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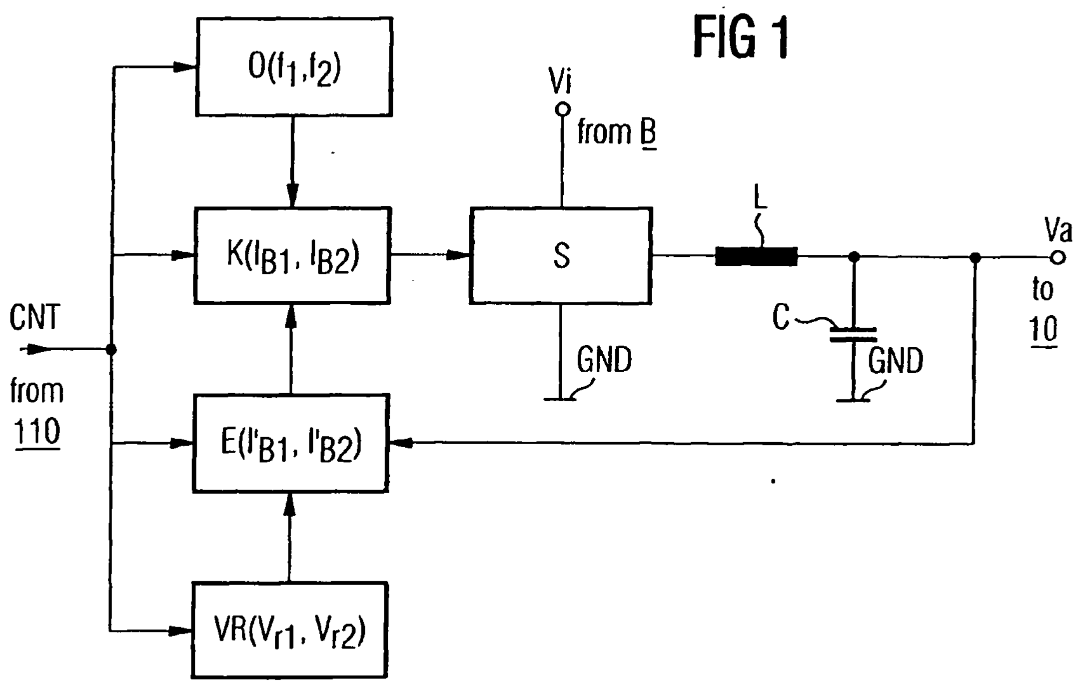
(54) A method and device for controlling the power consumption of a mobile radio device

(57) This invention provides a method for controlling the power consumption of a mobile radio device, in particular a mobile phone, having a pulse width modulation DC/DC-converter for converting a battery (B) supply voltage (V_i) to an internal supply voltage (V_o) for an internal electrical circuit (10) of said mobile radio device, said method comprising the steps of: providing at least one switchable component (O, K, E, VR) for said pulse width modulation DC/DC-converter, said least one switchable component (O, K, E, VR) having at least two switching states, a first switching state corresponding to a first output power requirement and a second switching state corresponding to a second output power requirement of said internal electrical circuit (10); deriving an internal logical control signal (CNT), said internal logical control signal (CNT) reflecting a first output power requirement operation period or a second output power requirement operation period of said internal electrical circuit (10); and switching said least one switchable component (O, K, E, VR) in accordance with said derived internal logical control signal (CNT).

FIG 1



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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a method and device for controlling the power consumption of a mobile radio device, and in particular a mobile phone, having a pulse width modulation DC/DC-converter for converting a battery supply voltage to an internal supply voltage for an internal electrical circuit of said mobile radio device.

[0002] Although applicable to any mobile radio devices, the present invention and its underlying problems will be discussed with particular reference to GSM mobile systems.

[0003] In present generations of mobile phones, DC/DC-converters are often used to generate an internal supply voltage for an associated internal electrical circuit, such as a digital part formed as an integrated circuit, in order to achieve the lowest possible current consumption, thus keeping the battery operation time as long as possible. This is especially beneficial, if the internal supply voltage is low compared to the battery supply voltage, i.e. in case of a DC/DC-downconverter.

[0004] Fig. 4 shows a simplified block diagram of a usual mobile phone having a pulse width modulation DC/DC-converter for converting a battery supply voltage to an internal supply voltage of a baseband digital part.

[0005] In Fig. 4 reference sign B denotes a battery, R1 a first voltage regulator, R2 a second voltage regulator, R3 a third voltage regulator, 10 a baseband digital part, 20 a baseband analog part, 30 a radio frequency part, 40 a transmitter, 50 an antenna, 60 a loudspeaker, and 70 a microphone.

[0006] The first voltage regulator R1 is pulse width modulation DC/DC-downconverter for downconverting a battery supply voltage to an internal supply voltage of the baseband digital part 10 which part is usually supplied with the lowest voltage present in the phone.

[0007] The second voltage regulator R2 for the baseband analog part 20 and the third voltage regulator R3 for the radio frequency 30 are linear regulators because of the low noise requirements of the analog circuits in the baseband analog part 20 and the radio frequency part 30, respectively.

[0008] The technical problem associated with the concept of the mobile phone shown in Fig. 4 is the large dynamic range of the load current for the baseband digital part 10 to be supplied by the first voltage regulator R1 in form of said pulse width modulation DC/DC-downconverter.

[0009] A typical situation is indicated in Fig. 5 which shows the load current of the baseband digital part 10 as a function of time for a GSM mobile phone in the standby state (a similar profile may be found in other mobile phone systems).

[0010] From Fig. 5 it can be seen that the power is drawn in very short load bursts of approximately 2 ms, typically spaced 0,5 - 2 s apart. The start of the bursts µP-on corresponds to the microprocessor starting its activity associated with the sychronization of the network and paging procedures which lead to a current consumption of the order of 20 - 50 mA. Once the microprocessor stops its activity, the digital baseband part 10 goes to sleep mode and the current drops very low to a value of the order of 200 µA as only a simple counter is running at a 32,768 kHz oscillator for counting up to the time of the next activity period.

[0011] With the demand of decreasing size of the mobile phones, also the components L and C of the pulse width modulation DC/DC-converter should be made physically minimized, i.e. their capacitance and inductance values be made lower. However, decreased capacitance and inductance values require an increased switching frequency in order to keep the output power constant.

[0012] On the other hand, a high switching frequency results in higher losses in the DC/DC-converter, leading to a lower power efficiency, especially at low loads.

[0013] Fig. 6 shows the efficiency loss of a typical DC/DC-converter as a function of the load current between 0 and 50 mA, and Fig. 7 as a function of the load current between 1 and 5 mA.

[0014] In Fig. 6 and 7, I_q denotes the quiescent current losses mainly originating from and being proportional to the bias currents of the comparator and error amplifier, I_f the switching losses being proportional to the frequency, and I_r the I^2R losses for a parasitic output resistance R.

[0015] As becomes readily apparent from Fig. 6 and 7, the quiescent current losses I_q and the switching losses I_f dominate at low output currents, i.e. in the sleep mode, while the I^2R losses I_r become comparable at high output currents, i.e. in the activity mode.

[0016] Today, various schemes are used to overcome this problem. Some of the most popular are often referred to as PFM (pulse frequency modulation), fixed on-time or fixed off-time. According to these schemes, the switching frequency is changed according to the load. This is achieved either by measuring the output current and adjusting the switching frequency accordingly (PFM), or by using a comparator which measures the output voltage to control the switch.

[0017] Both methods require increased circuit complexity compared to a fixed frequency PWM converter and both have decreased load regulation performance at low switching frequencies. The comparator controlled type furthermore involves a larger output ripple inherent to the nature of this control scheme.

SUMMARY OF THE INVENTION

[0018] The present invention provides a method and device for controlling the power consumption of a mobile radio device, and in particular a mobile phone, having a pulse width modulation DC/DC-converter for converting

a battery supply voltage to an internal supply voltage, as defined in independent claims 1 and 6, respectively.

[0019] The principal idea underlying the present invention is to use information available in the mobile radio device to change the operating mode of the DC/DC-converter in order to save power, thus improving the operation time of the device. The changeover of the operating mode from sleep mode to an active mode is controlled by an internal logical control signal. It is this control signal which according to the invention is also used to switch the DC/DC-converter from a low power requirement mode having a low PWM frequency to a high power requirement mode having a high PWM frequency, namely not as a reaction of a changing load current, but anticipating a changing load current.

[0020] A particular advantage is that the load regulation problem described above is eliminated. Furthermore, the circuit complexity is low, because existing information is used, thus preventing the need for load current sensing circuitry.

[0021] The mobile radio device, f.e. the mobile phone, has increased performance due to the fact that the efficiency of the DC/DC-converter can always be kept at optimum.

[0022] Preferred embodiments of the present invention are listed in the respective dependent claims.

[0023] According to a preferred embodiment, said at least one switchable component for said pulse width modulation DC/DC-converter is selected from among the group of: a switchable oscillator having at least two switchable frequencies, a comparator having a switchable bias current source having at least two switchable comparator bias currents, an error amplifier having a switchable bias current source having at least two switchable error amplifier bias currents, and a switchable error amplifier reference voltage source having at least two switchable error amplifier reference voltages. These are the essential power determining components of a conventional DC/DC converter.

[0024] According to a further preferred embodiment, said internal electrical circuit is a baseband digital part and said internal logical control signal is derived from a control logic of said baseband digital part.

[0025] According to a further preferred embodiment, said first switching state corresponds to a low output power requirement and said second switching state corresponds to a high output power requirement of said internal electrical circuit.

[0026] According to a further preferred embodiment, said internal logical control signal is used to changeover from a first low power low, frequency clock source to a second high power, high frequency clock source for said internal electrical circuit. This signal indicates the changeover between the sleep and traffic modes and is usually generated by an internal counter circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The present invention will become more fully understood by the following detailed description of preferred embodiments thereof in conjunction with the accompaying drawings, in which:

Fig. 1 a schematic diagram of a DC/DC-converter used in a first embodiment of the present invention;

Fig. 2 a schematic diagram of a DC/DC-converter used in a second embodiment of the present invention;

Fig. 3 the efficiency loss of the DC/DC-converter shown in Fig. 2 as a function of the load current between 1 and 5 mA;

Fig. 4 a simplified block diagram of a usual mobile phone having a pulse width modulation DC/DC-converter for converting a battery supply voltage to an internal supply voltage of a baseband digital part;

Fig. 5 the load current of the baseband digital part 10 as a function of time for said mobile phone in the standby state;

Fig. 6 the efficiency loss of a typical DC/DC-converter as a function of the load current between 0 and 50 mA;

Fig. 7 the efficiency loss of a typical DC/DC-converter as a function of the load current between 1 and 5 mA; and

Fig. 8 an usual baseband digital part for a mobile phone adapted to employ a two clock source scheme.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] In the figures, the same reference signs denote the same or functionally equivalent elements.

[0029] Fig. 8 shows an usual baseband digital part for a mobile phone adapted to employ a two clock source scheme.

[0030] In Fig. 8, reference sign 80 denotes a 32,768 kHz oscillator and 100 is a 13 MHz oscillator.

[0031] The following components of the baseband digital part 10 are specifically denoted: a real time clock 120, a clock source switch 130, a control logic 110, a control signal CNT from the control logic 110, and the digital core 150.

[0032] The 13 MHz oscillator 100 is the main clock source and comprised of a high accuracy, high frequen-

cy oscillator. This main clock source is used whenever the mobile phone is in active or traffic mode, i.e. connected to the network, or when the software tasks require more processing power, f.e. MMI functions etc. In periods of low activity, the clock source is changed to the ultra low power, low frequency clock in form of the 32,768 kHz oscillator 80 in order to save power whose frequency is adapted to accomodate real clock functions.

[0033] The changeover of the clock source is controlled by the logical control signal CNT which enables/disables the 13 MHz oscillator 100 and simultaneously changes the switch position of the clock source switch 130. In other words, the 13 MHz oscillator 100 is only active in traffic mode periods, whereas the 32,768 kHz oscillator 80 is always kept turned on because of its ultra low power consumption.

[0034] Thus, said internal logical control signal CNT controls a first low output power requirement operation period and a second high output power requirement operation period of said baseband digital part 10.

[0035] Fig. 1 shows a schematic diagram of a DC/DC-converter used in a first embodiment of the present invention.

[0036] In Fig. 1, reference sign O denotes a switchable oscillator having a first and second frequency f_1, f_2, K a switchable comparator having a first and second bias current I_{B1}, I_{B2}, E a switchable error amplifier having a first and second bias current I'_{B1}, I'_{B2}, VR a switchable voltage reference having a first and second reference voltage V_{r1}, V_{r2}, S a switch, V_i a battery supply voltage, V_o an output voltage, L an inductance, C a capacitance, and GND ground or earth potential.

[0037] In this embodiment, the switching of said switchable components O, K, E, VR of the DC/DC converter is performed in accordance with said internal logical control signal CNT derived from the control logic 110. Thus, it is not necessary to react to a change in output power sensed at the output of the DC/DC-converter, but the change in required power can be anticipated by having the signal CNT.

[0038] Here, the switchable components O, K, E, VR have two switching states, a first switching state (index "1") corresponding to a first low output power requirement and a second switching state (index "2") corresponding to a second high output power requirement of said baseband digital part 10.

[0039] In the sleep mode, all switching states are set to first switching state effecting low power consumption, and in the traffic mode, all switching states are set to second switching state effecting relatively high power consumption.

[0040] As becomes readliy apparent to the average skilled person, low values of switching frequency, bias currents and reference voltage (determines output voltage) imply a low power consumption and vice versa high values of switching frequency, bias currents and reference voltage (determines output voltage) imply a high power consumption.

[0041] Thus, each of these parameters can be optimized for the respective operation mode.

[0042] Fig. 2 shows a schematic diagram of a DC/DC-converter used in a second embodiment of the present invention.

[0043] In Fig. 2, reference sign FS indicates a frequency select input, FF a PWM latch, IBK a bias current source for the comparator K, IBE a bias current source for the error amplifier E, T1 a top side switching transistor, T2 a synchronous transistor rectifier, and V_r a reference voltage.

[0044] In comparison to Fig. 1, in the embodiment shown in Fig. 2 some more electrical circuit details will be explained. Thus, the battery supply voltage V_i typically amounts to 3 - 5,5 volts, whereas the output voltage V_o typically amounts to 1,8 volts.

[0045] The switch S of Fig. 1 has been realized as the synchronizing latch and the two transistors T1, T2. No switching of the reference voltage determining the magnitude of the output voltage V_o is provided in this example.

[0046] The control signal CNT provided by the control logic 110 which is used to power down the 13 Mhz frequency clock 100, is used to shift the frequency of the oscilllator O of the DC/DC converter and to decrease the bias currents of the bias current sources IBK and IBE, respectively.

[0047] Fig. 3 shows the efficiency loss of the DC/DC-converter shown in Fig. 2 as a function of the load current between 1 and 5 mA.

[0048] The data shown in Fig. 3 were obtained by lowering the switching frequency of the oscillator O from 256 kHz in the active mode to 32 kHz in the sleep mode and decreasing the quiescent current of the comparator K and the error amplifier from 200 µA to 50 µA. The improvement becomes obvious from a comparison with Fig. 7 which shows the results of the conventional device using a single switching frequency and fixed quiescent currents.

[0049] Although the present invention has been described with respect to preferred embodiments thereof, it should be understood that many modifications can be performed without departing from the scope of the invention as defined by the appended claims.

[0050] Particularly, the switchable parameters of the DC/DC converter and the internal logical control signal can have more than two discrete values.

[0051] Moreover, not all of the four parameters mentioned in the above example have to be changed. For example, there may be applications where it is not permissible to alter the output voltage in the sleep mode. In more complicated designs of the DC/DC converter, there may be additional parameters to be switched.

[0052] Also, the control signal may be derived from another component within the mobile radio device, and not only from the baseband digital part.

Claims

1. A method for controlling the power consumption of a mobile radio device, in particular a mobile phone, having a pulse width modulation DC/DC-converter for converting a battery (B) supply voltage (V_i) to an internal supply voltage (V_o) for an internal electrical circuit (10) of said mobile radio device, said method comprising the steps of:

   providing at least one switchable component (O, K, E, VR) for said pulse width modulation DC/DC-converter, said least one switchable component (O, K, E, VR) having at least two switching states, a first switching state corresponding to a first output power requirement and a second switching state corresponding to a second output power requirement of said internal electrical circuit (10);

   deriving an internal logical control signal (CNT), said internal logical control signal (CNT) reflecting a first output power requirement operation period or a second output power requirement operation period of said internal electrical circuit (10); and

   switching said least one switchable component (O, K, E, VR) in accordance with said derived internal logical control signal (CNT).

2. The method according to claim 1, wherein said at least one switchable component (O, K, E, VR) for said pulse width modulation DC/DC-converter is selected from among the group of:
   a switchable oscillator (O) having at least two switchable frequencies (f_1, f_2), a comparator (K) having a switchable bias current source having at least two switchable comparator bias currents (I_{B1}, I_{B2}), an error amplifier(E) having a switchablebias current source having at least two switchable error amplifier bias currents (I'_{B1}, I'_{B2}), and a switchable error amplifier reference voltage source (VR) having at least two switchable error amplifier reference voltages (V_{r1}, V_{r2}).

3. The method according to claim 1 or 2, wherein said internal electrical circuit (10) is a baseband digital part and said internal logical control signal (CNT) is derived from a control logic (110) of said baseband digital part.

4. The method according to claim 1, 2 or 3, wherein said first switching state corresponds to a low output power requirement and said second switching state corresponds to a high output power requirement of said internal electrical circuit (10).

5. The method according to of the preceeding claims, wherein said internal logical control signal (CNT) is used to changeover from a first low power low, frequency clock source (80) to a second high power, high frequency clock source (100) for said internal electrical circuit (10).

6. A device for controlling the power consumption of a mobile radio device, in particular a mobile phone, having a pulse width modulation DC/DC-converter for converting a battery supply voltage to an internal supply voltage for an internal electrical circuit of said mobile radio device, said device comprising:

   at least one switchable component (O, K, E, VR) of said pulse width modulation DC/DC-converter, said least one switchable component (O, K, E, VR) having at least two switching states, a first switching state corresponding to a first output power requirement and a second switching state corresponding to a second output power requirement of said internal electrical circuit (10);

   a derivation means for deriving an internal logical control signal (CNT), said internal logical control signal (CNT) reflecting a first output power requirement operation period or a second output power requirement operation period of said internal electrical circuit (10); and

   a switching means for switching said least one switchable component (O, K, E, VR) in accordance with said derived internal logical control signal (CNT).

7. The device according to claim 6, wherein said at least one switchable component (0, K, E, VR) for said pulse width modulation DC/DC-converter is selected from among the group of:
   a switchable oscillator (O) having at least two switchable frequencies (f_1, f_2), a comparator (K) having a switchable bias current source having at least two switchable comparator bias currents (I_{B1}, I_{B2}), an error amplifier(E) having a switchablebias current source having at least two switchable error amplifier bias currents (I'_{B1}, I'_{B2}), and a switchable error amplifier reference voltage source (VR) having at least two switchable error amplifier reference voltages (V_{r1}, V_{r2}).

8. The device according to claim 6 or 7, wherein said internal electrical circuit (10) is a baseband digital part and said internal logical control signal (CNT) is derived from a control logic (110) of said baseband digital part.

9. The device according to claim 6, 7 or 8, wherein said

first switching state corresponds to a low output power requirement and said second switching state corresponds to a high output power requirement of said internal electrical circuit (10).

10. The device according to one of claim 6 to 9, wherein said internal logical control signal (CNT) effects a changeover from a first low power low, frequency clock source (80) to a second high power, high frequency clock source (100) for said internal electrical circuit (10).

FIG 1

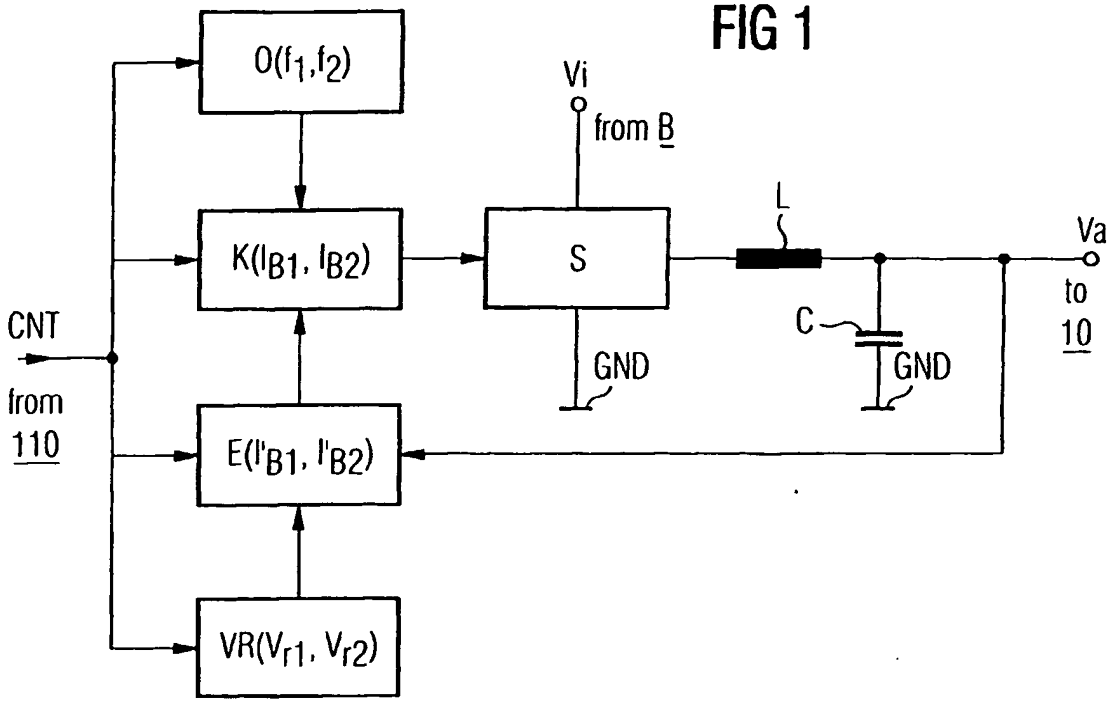

O(f1,f2)
Vi
from B
K(IB1, IB2)
S
L
Va
to
10
CNT
from
110
C
GND
GND
E(I'B1, I'B2)
VR(Vr1, Vr2)

FIG 2

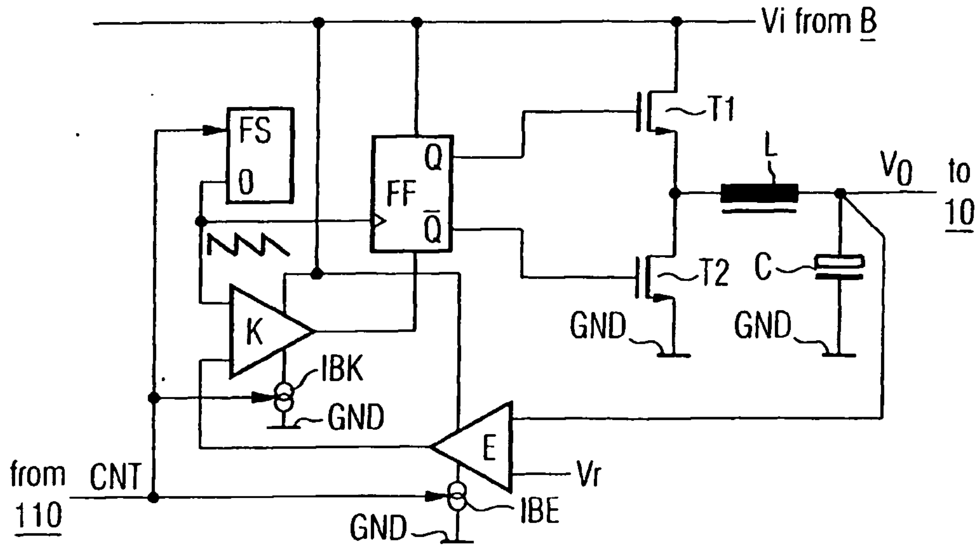
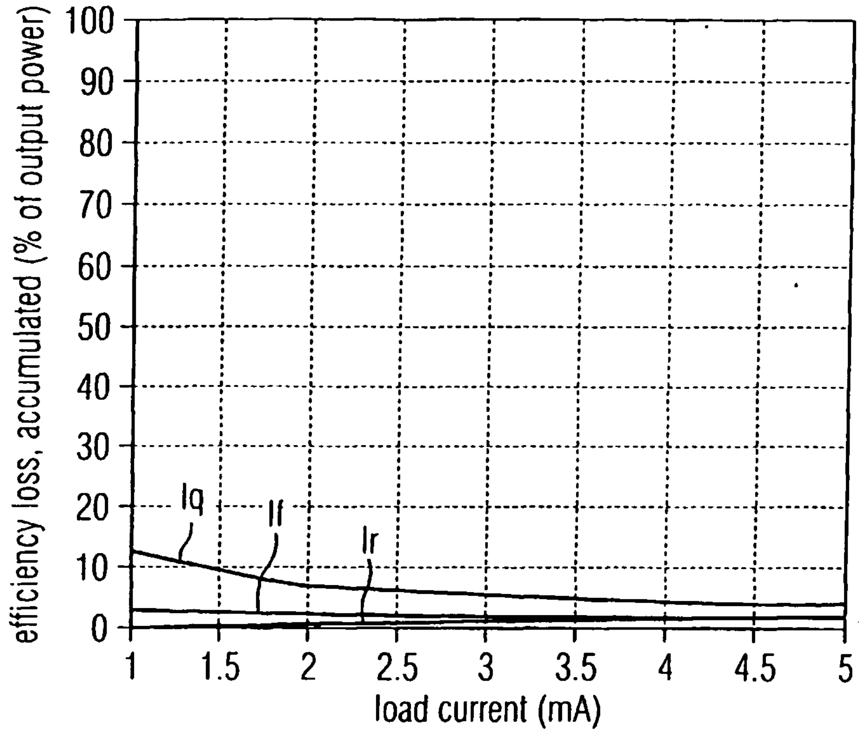
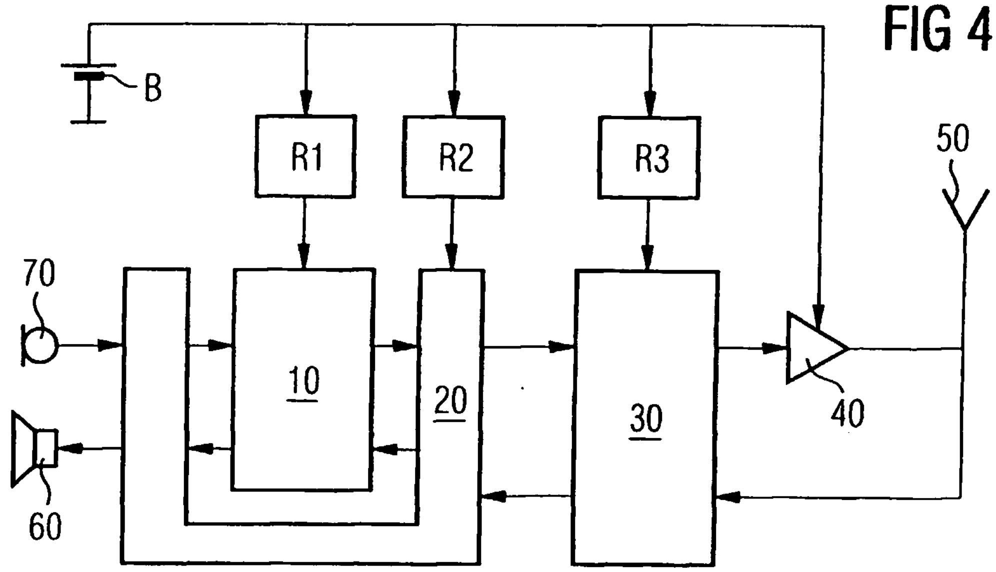

Vi from B
FS
0
Q
FF
Q
T1
L
V0
to
10
T2
C
GND
GND
K
IBK
GND
E
Vr
from
110
CNT
IBE
GND

FIG 3



efficiency loss, accumulated (% of output power)
100
90
80
70
60
50
40
30
20
10
0
Iq
If
Ir
1
1.5
2
2.5
3
3.5
4
4.5
5
load current (mA)

FIG 4



B
R1
R2
R3
50
70
10
20
30
40
60

FIG 5

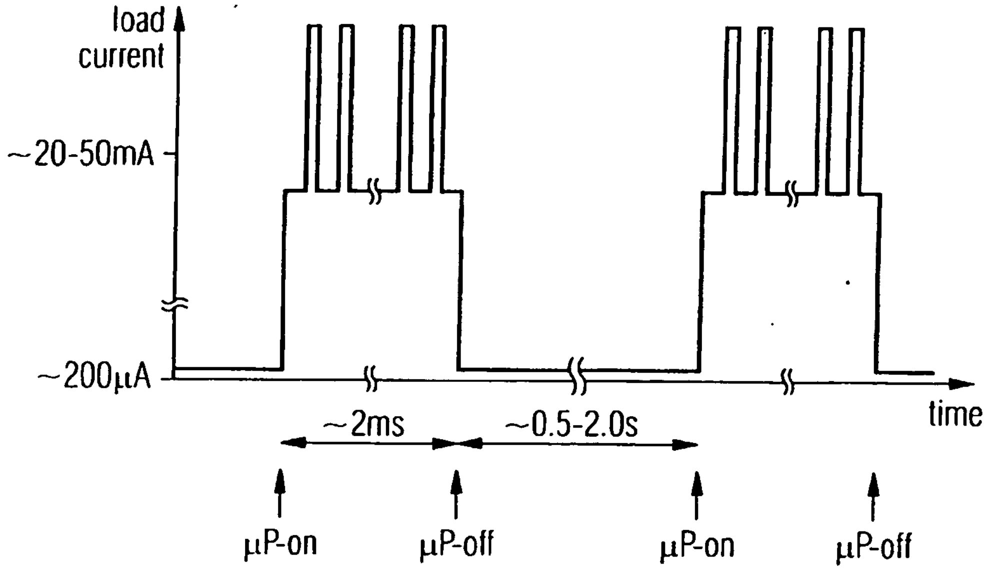

load
current
~20-50mA
~200µA
time
~2ms
~0.5-2.0s
µP-on
µP-off
µP-on
µP-off

FIG 6

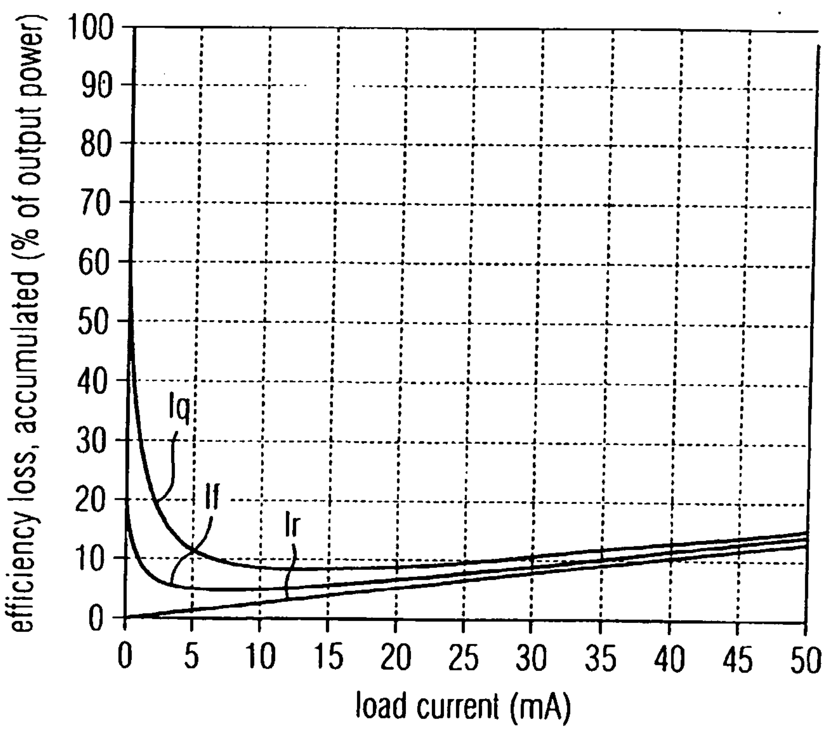

efficiency loss, accumulated (% of output power)
100
90
80
70
60
50
40
30
20
10
0
Iq
If
Ir
0
5
10
15
20
25
30
35
40
45
50
load current (mA)

FIG 7

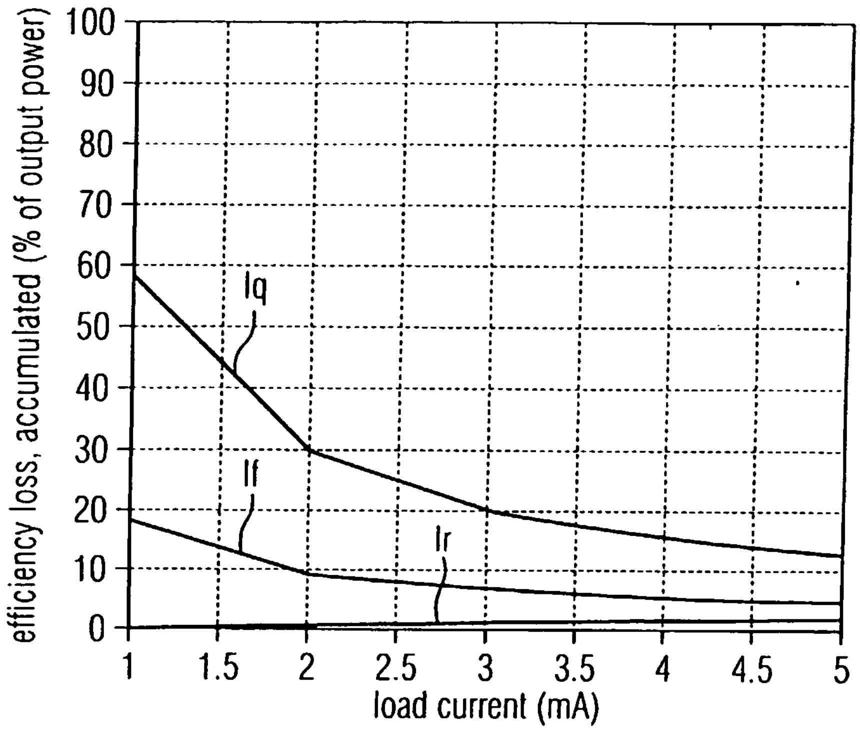
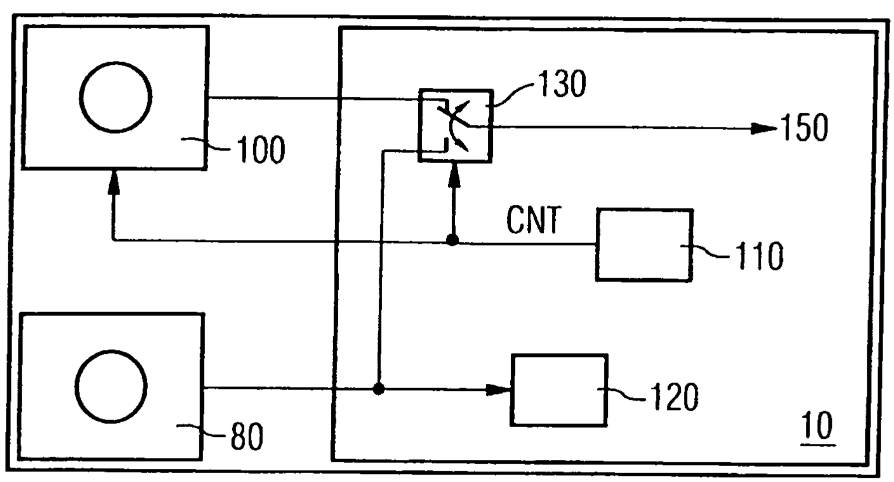

efficiency loss, accumulated (% of output power)
100
90
80
70
60
50
40
30
20
10
0
Iq
If
Ir
1
1.5
2
2.5
3
3.5
4
4.5
5
load current (mA)

FIG 8


130
150
100
CNT
110
120
80
10

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EUROPEAN SEARCH REPORT

Application Number
EP 98 12 0284

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	GB 2 284 085 A (NIPPON ELECTRIC CO) 24 May 1995 * the whole document *	1,2,4,6,7,9	H04B1/16
X A	US 5 274 369 A (TSUNODA KAZUYUKI ET AL) 28 December 1993 * abstract; figures 1,3 * * column 4, line 8 - column 5, line 14 * * column 8, line 51 - line 59 *	1,6 2-5,7-10	
A	DE 195 45 659 A (THOMSON BRANDT GMBH) 12 June 1997 * abstract; claim 1; figure 1 *	1-10	
A	US 4 688 159 A (MARINUS ANTONIUS A M) 18 August 1987 * abstract; claim 1; figure 1 *	1-10	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H04B
H02M
H04Q

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	23 February 1999	Kolbe, W

CATEGORY OF CITED DOCUMENTS

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23-02-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2284085 A	24-05-1995	JP 7143050 A	02-06-1995
		KR 9707984 B	19-05-1997
		US 5821738 A	13-10-1998
US 5274369 A	28-12-1993	GB 2242049 A,B	18-09-1991
		HK 86197 A	27-06-1997
		JP 2754928 B	20-05-1998
		JP 4211528 A	03-08-1992
DE 19545659 A	12-06-1997	NONE	
US 4688159 A	18-08-1987	NL 8502338 A	16-03-1987
		CN 1005602 B	25-10-1989
		EP 0214680 A	18-03-1987
		JP 62048265 A	02-03-1987
		KR 9604259 B	28-03-1996
		US 4766528 A	23-08-1988

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